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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,668	12/19/2000	Akira Nonaka	450100-02904	7062

20999 7590 02/16/2005

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EXAMINER	
DAVIS, ZACHARY A	

ART UNIT	PAPER NUMBER
2137	

DATE MAILED: 02/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,668	NONAKA ET AL.	
	Examiner	Art Unit	
	Zachary A Davis	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,15-22 and 57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,15-22 and 57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20041028*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. An amendment was received on 08 September 2004. Claims 1, 5, 7, 10, and 17 have been amended. Claims 12-14 and 23-56 have been canceled. New Claim 57 has been added. Claims 1-11, 15-22, and 57 are currently pending in the present application.

Information Disclosure Statement

2. An Information Disclosure Statement was received on 28 October 2004. The submission is in compliance with the provisions of 37 CFR 1.97 and has therefore been considered.

Specification

3. The disclosure is objected to because of the following informalities: The amendment to the specification was intended to correct the reference to "I2C interface 1130" to refer instead to "I2C interface 1134". However, this change was not made, and the change was instead made to alter the reference to "medium SAM interface 1131" to read "medium SAM interface 1134". Appropriate correction is required.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 101

Claim Rejections - 35 USC § 112

5. The rejection of Claims 5-7 and 10 under 35 U.S.C. 112, second paragraph, as being indefinite, is withdrawn in light of the amendment to the claims. The rejections of Claims 17-22 under 35 U.S.C. 101 as being directed to non-statutory subject matter and under 35 U.S.C. 112, second paragraph, as being indefinite, are withdrawn in light of Applicant's arguments.

Response to Arguments

6. Applicant's arguments filed 08 September 2004 have been fully considered but they are not persuasive.

Regarding amended independent Claims 1 and 17, Applicant acknowledges the Examiner's previous statement that Schneier, US Patent 5768382, does not explicitly disclose determining a mode based on handling policy. Applicant further acknowledges the use of Christiano, US Patent 5671412, to remedy this deficiency. However, Applicant argues that Christiano does not disclose an equivalent to the purchase modes recited in, for example, Claims 1 and 17. The Examiner respectfully disagrees. It is

noted that the cited portion of Applicant's specification (page 101, lines 2-12) describes the purchase modes in exemplary terms, which is therefore not a limiting definition. Thus the Examiner believes that Christiano does disclose a mode which is used in creating usage control status data that is used to control the use of content to what is allowed within the limits of the mode (see column 7, lines 20-23, where, for example, a predetermined number of uses of the licensed content or a predetermined amount of time for using the licensed content are allowed; see also column 10, line 53-column 11, line 11, where it is determined whether use of the licensed content is allowed based on the status of the license).

Therefore, the claims are rejected as set forth below.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim 57 is rejected under 35 U.S.C. 102(b) as being anticipated by Christiano, US Patent 5671412.

Christiano discloses a method including determining a usage or purchase mode based on a usage license policy (column 6, line 60-column 7, line 30), creating log data (column 18, lines 53-61), creating usage control status data (column 10, lines 53-57),

controlling use of content data (column 10, line 64- column 11, line 3), recording the content data (column 10, lines 62-64, where the product is used on a computer system, and therefore stored at least temporarily therein; see also column 6, lines 28-31where various storage media are disclosed), and encrypting key data and control data (column 14, lines 23-28).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-10 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneier, US Patent 5768382, in view of Christiano, US Patent 5671412.

In reference to Claim 1, Schneier discloses an apparatus within a tamper-resistant circuit module (column 8, lines 17-27; column 11, lines 31-37) including a first bus (see Figures 4C-4H), an arithmetic processing circuit (Figure 4C, CPU 302), a storage circuit (Figure 4C, ROM 304), a second bus (see Figures 4C-4H), an interface circuit (see Figure 4C), an encryption processing circuit (Figure 4B-4C, encryption/decryption module 28; also column 11, lines 41-46), and an external bus interface circuit (Figure 4C, I/O 312). However, Schneier does not explicitly disclose

determining a mode based on a handling policy and creating log data, nor does Schneier disclose creating usage control status data or controlling the use of the content data.

Christiano discloses determining a usage or purchase mode based on a usage license policy (column 6, line 60-column 7, line 30) and logging data (column 18, lines 53-61). Christiano further discloses creating usage control status data (column 10, lines 53-57) and controlling use of content data (column 10, line 64- column 11, line 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the apparatus of Schneier by including the usage policies and licensing as disclosed by Christiano, in order to provide a variety of options and flexibility in controlling usage of licensed data (see Christiano, column 3, lines 12-19).

In reference to Claim 2, Schneier further discloses a second interface circuit and that the first bus includes a third bus and a fourth bus (see Figures 4C-4H).

In reference to Claim 3, Schneier further discloses a third interface circuit communicating with a recording medium (Figure 4H, interface circuitry 406), a fifth bus, and a fourth interface circuit (see Figures 4C-4H).

In reference to Claim 4, Schneier further discloses a public key encryption circuit (column 10, lines 27-56) and a common key encryption circuit (column 9, line 62-column 10, line 11).

In reference to Claim 5, Schneier further discloses that the storage circuit stores private and public key data (column 11, lines 44-48), the public key encryption circuit

verifies the integrity of signature data and creates signature data (column 10, lines 41-56), and the common key encryption circuit encrypts and decrypts content data and key data using a session key (column 9, line 65-column 10, line 6).

In reference to Claim 6, Schneier further discloses a hash value generating circuit used by the public key encryption circuit in verifying and creating signatures (column 17, lines 46-50).

In reference to Claim 7, Schneier further discloses a random number generating circuit (column 10, lines 57-67).

In reference to Claim 8, Schneier further discloses an external storage circuit (column 7, lines 57-60).

In reference to Claims 9 and 11, Schneier and Christiano disclose everything as applied to Claim 8 above. Schneier further discloses that programs are executed from memory in a conventional manner (column 7, lines 60-61). However, Schneier does not explicitly disclose a storage-circuit control circuit or a storage management circuit. Official notice is taken that it is well known in the computer arts to include a memory controller or memory management circuit, such as a DMA or MMU, in order to allow for the optimization of the use of memory. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the apparatus of Schneier and Christiano by including a memory controller or manager, in order to optimize the use of memory, as is well known in the computer arts.

In reference to Claim 10, Schneier further discloses that the external bus is connected to a host processor (see Figure 4C, where the I/O 312 is connected to external CPU 27).

In reference to Claim 15, Schneier further discloses a real time clock (column 11, line 46). Further, Christiano discloses encrypting key data and control data (column 14, lines 23-28) and storing license key data (column 14, lines 19-21).

In reference to Claim 16, Schneier further discloses that the storage circuit writes and erases data in units of blocks and also discloses a write lock control circuit for controlling writing and erasing blocks of data (column 18, lines 39-43).

In reference to Claim 17, Schneier discloses an apparatus within a tamper-resistant circuit module (column 8, lines 17-27; column 11, lines 31-37) including a first bus (see Figures 4C-4H), an arithmetic processing circuit (Figure 4C, CPU 302), a storage circuit (Figure 4C, ROM 304), a second bus (see Figures 4C-4H), an interface circuit (see Figure 4C), an encryption processing circuit (Figure 4B-4C, encryption/decryption module 28; also column 11, lines 41-46), and an external bus interface circuit (Figure 4C, I/O 312). Schneier further discloses receiving an interrupt from an external circuit, performing processing, and reporting a result of the processing (column 11, lines 55-67). However, Schneier does not explicitly disclose determining a mode based on a handling policy and creating log data, nor does Schneier disclose creating usage control status data or controlling the use of the content data.

Christiano discloses determining a usage or purchase mode based on a usage license policy (column 6, line 60-column 7, line 30) and logging data (column 18, lines 53-61). Christiano further discloses creating usage control status data (column 10, lines 53-57) and controlling use of content data (column 10, line 64- column 11, line 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the apparatus of Schneier by including the usage policies and licensing as disclosed by Christiano, in order to provide a variety of options and flexibility in controlling usage of licensed data (see Christiano, column 3, lines 12-19).

11. Claims 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneier in view of Christiano as applied to claim 17 above, and further in view of Castor et al, US Patent 5590288.

In reference to Claims 18 and 19, Schneier and Christiano disclose everything as applied to Claim 17 above. However, Schneier as modified above does not explicitly disclose reporting the result of processing by outputting an interrupt. Further, Schneier as modified above does not explicitly disclose that the external bus interface includes a common memory and that the external circuit obtains a result by polling.

Castor discloses a system which allows a computer to request another computer to execute a procedure (column 3, lines 38-42) including outputting an interrupt (column 12, lines 29-33). Castor further discloses a common memory (the buffer of column 12, lines 33-35) and polling an interface circuit to obtain a result (column 12, lines 35-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the apparatus of Schneier and Christiano by including the interrupt, buffer, and polling of Castor, in order to increase reliability, lower cost, and allow easier upgrades in a distributed computing system (Castor, column 4, lines 11-21).

In reference to Claim 20, Castor further discloses first status registers including flags (column 12, lines 29-35).

In reference to Claim 21, Castor further discloses storing and executing an interrupt program (column 5, lines 49-51).

In reference to Claim 22, Castor further discloses storing and executing a plurality of interrupt programs and subroutines (column 5, lines 49-55).

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zachary A Davis whose telephone number is (571) 272-3870. The examiner can normally be reached on weekdays 8:30-6:00, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on (571) 272-3868. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ZAD
zad

ANDREW CALDWELL
SUPERVISORY PATENT EXAMINER